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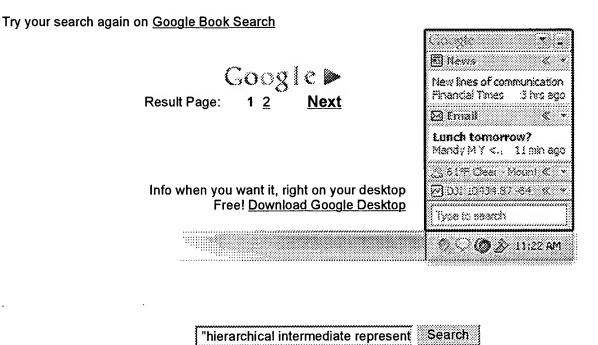
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S Gupta, N Dutt, R Gupta, A Nicolau - IEE PROCEEDINGS COMPUTERS AND DIGITAL TECHNIQUES, 2003 - ieeexplore.ieee.org

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2.2.1 Winning Hierarchical Intermediate Representation (WHIRL) ...

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... intermediate representation of a service design, it also calculates the

design's cost, which is the sum of the cost of the components ...

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We define a hierarchical task graph as follows: Definition 4.1. ...

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Albert Cohen, Marc Sigler, Sylvain Girbal, Olivier Temam, David Parello, Nicolas Vasilache June 2005 Proceedings of the 19th annual international conference on **Supercomputing ICS '05**

Publisher: ACM Press

Full text available; mpdf(365.49 KB) Additional Information; full citation, abstract, references

Static compiler optimizations can hardly cope with the complex run-time behavior and hardware components interplay of modern processor architectures. Multiple architectural phenomena occur and interact simultaneously, which requires the optimizer to combine multiple program transformations. Whether these transformations are selected through static analysis and models, runtime feedback, or both, the underlying infrastructure must have the ability to perform long and complex compositions of progra ...

Coordinated parallelizing compiler optimizations and high-level synthesis



Sumit Gupta, Rajesh Kumar Gupta, Nikil D. Dutt, Alexandru Nicolau October 2004 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 9 Issue 4

Publisher: ACM Press

Full text available: pdf(923.65 KB) Additional Information: full citation, abstract, references, index terms

We present a high-level synthesis methodology that applies a coordinated set of coarsegrain and fine-grain parallelizing transformations. The transformations are applied both during a pre-synthesis phase and during scheduling, with the objective of optimizing the results of synthesis and reducing the impact of control flow constructs on the quality of results. We first apply a set of source level presynthesis transformations that include common sub-expression elimination (CSE), copy propagat ...

Keywords: Code motions, common subexpression elimination, dynamic CSE, embedded systems, high-level synthesis, parallelizing transformations, presynthesis

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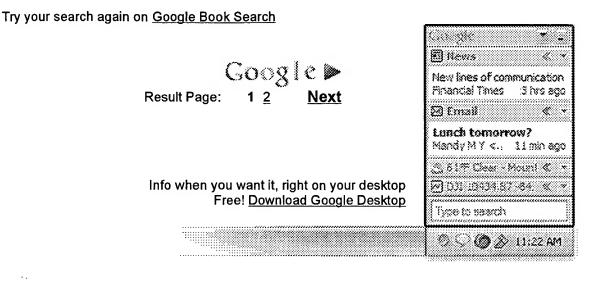
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9	BRS	L9	1	"6662356".pn. and processing	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 18:10
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12	BRS	L12	3	(compiler) and (suspend adj processing) and (resume adj processing) and thread	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 18:12
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33	BRS	L41	1	"6662356".pn. and block	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:18
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36	BRS	L44	0	(new adj binary adj code) and (first adj program) and (jump near instruction\$2) and (interal adj representation)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:20
37	BRS	L45	0	(new adj binary adj code) and (first adj program) and (jump near instruction\$2)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:20
38	BRS	L46	1	"6662356".pn. and jump	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:30
39	BRS	L47	1	"6662356".pn. and second	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:33
40	BRS	L48	1	"6662356".pn. and flow	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/15 19:51

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